I. AMENDMENTS TO THE CLAIMS:

Please cancel claims 12-20 without prejudice. Kindly amend claim 11 as follows.

The present listing of claims replaces all prior listings, or versions, of claims in the present application.

LISTING OF CLAIMS:

1. (Previously Presented) A Secure Digital Input Output controller having a single-chip semiconductor device connecting a Secure Digital Input Output-compliant Secure Digital Input Output host device with a plurality of applications via a Secure Digital bus, comprising:

(a) a Secure Digital interface operably connectable with the Secure Digital Input Output host device to decode commands received from the Secure Digital Input Output host device, and to return a response to the Secure Digital Input Output host device;

(b) application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface;

(c) a temporary memory operably connected between the Secure Digital interface and application interfaces; and

(d) a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces.

2. (Previously Presented) A Secure Digital Input Output controller according to claim 1, wherein the temporary memory comprises a First-in, First-out device.

3. (Cancelled)

4. (Previously Presented) A Secure Digital Input Output controller according to claim 1,

wherein the temporary memory in the Secure Digital Input Output controller comprises as many read memories as the number of application interfaces to temporarily hold data read out of Secure Digital Input Output applications; and at least one write memory operably connected to temporarily hold data to be sent out from the Secure Digital Input Output host.

5. (Previously Presented) A Secure Digital Input Output controller according to claim 4, wherein each read memory is a First-in, First-out device and the write memory is a First-in, First-out device.

6. (Previously Presented) A Secure Digital Input Output controller according to claim 1, wherein the temporary memory in the Secure Digital Input Output controller comprises at least one read First-in, First-out device operably connected to temporarily hold data read out of Secure Digital Input Output applications; and at least one write First-in, First-out device operably connected to temporarily hold data to be sent out from the Secure Digital Input Output host.

7. (Cancelled)

8. (Previously Presented) A Secure Digital Input Output controller according to claim 1, further comprising a microcontroller unit for data control, wherein the microcontroller unit is connected to control the Secure Digital interface and application interfaces.

9. (Previously Presented) A Secure Digital Input Output controller according to claim 8, further comprising an Input/Output device connected to input and output control signals to and from the microcontroller unit.

10. (Previously Presented) A Secure Digital Input Output controller according to claim 9, wherein the Input/Output device is a general peripheral Input/Output device.

11. (Currently Amended) A Secure Digital Input Output controller according to claim 10, wherein the microcontroller unit operates to decode data when the data sent from the Secure Digital Input Output host device to the Secure Digital Input Output controller via the Secure Digital bus contains at least a register read/write address, a selected type of operation, a quantity of data, and ~~arbitrary~~ write data in a digital system, and the microcontroller unit operates to access non-contiguous registers via an application interface.

Claims 12 to 20 have been cancelled.

21. (Previously Presented) A Secure Digital Input Output controller according to claim 1, wherein the temporary memory comprises one First-in, First-out device for writing data and three First-in, First-out devices for reading data.